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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/980,974	03/06/2002	Karsten Jensen	1406/24	3607

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/980,974	JENSEN ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002 and 10 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) __ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on __ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/10/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.

(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, and 4-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Stallings, William, "Computer Organization and Architecture", 1996, Prentice-Hall, Inc., 4th edition, pages 9, 52, and 361-368 , (hereafter referred to as Stallings).

Referring to claim 1, Stallings discloses, as claimed, a method for branching when a program is executed by a processor

(see Fig. 3.2), where the program is stored in a program memory (the portion of Memory storing instruction, see Fig. 3.2) , and a variable memory (the portion of Memory storing Data, see Fig. 3.2) and a table memory (the other portion of Memory storing Data, see Fig. 3.2) for storing fixed values are provided, the processor executing the following steps:

a) a first memory cell (the memory cell saves (A) value, see page 367, lines 28-41, when the postindexing addressing mode is used wherein EA =(A) + (R)) in the variable memory (the portion of Memory storing Data, see Fig. 3.2) is addressed (by the address A, see page 367, lines 39-40),

b) a second memory cell (at the address EA saving the address value (EA) see indirect addressing mode in Fig. 10.1 or page 364, lines 12-36) in the variable memory (the portion of Memory storing Data, see Fig. 3.2) is addressed on the basis of the content ((A) value since EA =(A) + (R))of the first memory cell addressed in step a), and further parameters ((R) value in the index register since EA =(A) + (R)),

c) a memory cell (at the address (EA) saving the address value ((EA)) see indirect addressing mode in Fig. 10.1 or page 364, lines 12-36) in the table memory is addressed on the basis of the content (the address value (EA), see indirect addressing

mode in Fig. 10.1 or page 364, lines 12-36) of the second memory cell, addressed in step b), and

d) execution branches to a program address (at address ((EA)) of the program memory (the portion of Memory storing instruction, see Fig. 3.2), note this is in the situation when the address (EA) is used to reference the variable memory cell saving the address value of ((EA))) which is stored in that memory cell in the table memory (the other portion of Memory storing Data, see Fig. 3.2) which was addressed in step c).

As to claim 2, Stallings also discloses: the second memory cell in the variable memory is addressed (at the address EA =(A) + (R)) by the result of an instruction which processes the content of the first memory cell (the memory cell saves (A) value) in the variable memory and further parameters ((R) value in the index register since EA =(A) + (R)).

As to claim 4, Stallings also discloses an apparatus where the program memory (the portion of Memory storing instruction, see Fig. 3.2) is connected to the processor by means of a bidirectional bus (System Interconnection which certainly is a bidirectional bus see Fig. 1.4), an addressing unit (inside CPU see Fig. 3.2) is provided which receives first addresses (address value (A)) from the processor via a bus and converts the first addresses into second addresses (address value EA,

using adder for the ADD operation of EA =(A) + (R)), and thus uses a bus (System Interconnection, see Fig. 1.4) to address the variable memory (the portion of Memory storing Data, see Fig. 3.2), which can be read by the processor via a bus (System Interconnection, see Fig. 1.4), and the table memory is connected to the processor by means of a bidirectional bus (System Interconnection which certainly is a bidirectional bus see Fig. 1.4).

As to claim 5, Stallings also discloses: a device is provided which receives data from the variable memory (the portion of Memory storing Data, see Fig. 3.2) via a bus (System Interconnection, see Fig. 1.4) and receives data from the processor via a bus (System Interconnection, see Fig. 1.4), and uses the received data to calculate (using adder for the ADD operation of EA =(A) + (R)) an address for addressing the variable memory via a bus (System Interconnection, see Fig. 1.4).

As to claim 6, Stallings also discloses: the variable memory (the portion of Memory storing Data, see Fig. 3.2) is a read/write memory.

As to claim 7, Stallings also discloses: the table memory (the other portion of Memory storing Data, see Fig. 3.2) is a read/write memory.

As to claim 8, Stallings also discloses: the processor (CPU see Fig. 3.2) is in the form of an I/O processor (since the CPU shown in Fig. 3.2 can handle I/O operations for the peripherals thereof, see I/O AR and I/O BR in Fig. 3.2) for protocol processing.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stallings in view of Tanenbaum, Andrew S., "Modern Operating Systems", 1992, Prentice-Hall, Inc., pages 128-130, (hereafter referred to as Tanenbaum)

Stallings discloses the claimed invention except for: the variable memory is addressed using a first bit length a, and the table memory is addressed using a second bit length b, the first bit length a and the second bit length b being of different size.

Stallings shows, as set forth above, a program memory (the portion of Memory storing instruction, see Fig. 3.2), a variable memory (the portion of Memory storing Data, see Fig. 3.2) and a table memory (the other portion of Memory storing Data, see Fig. 3.2). The variable memory data may bump into the data in program memory or table memory during the execution of process in the Stallings's system (see Fig. 3-35 in Tanenbaum).

Tanenbaum shows that it is well know in the art to use separate segments (see Fig. 3-36) for storing different data in order to allow each data in its memory segment to grow or shrink independently of the other data. Further, it is well known in the art that the bit length used for addressing a memory is related to the size of the memory in order to save the address bits.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Stallings's system to comprise the variable memory is addressed using a first bit length a, and the table memory is addressed using a second bit length b, the first bit length a and the second bit length b being of different size, as taught by Tanenbaum, in order to prevent the variable memory data from bumping into the data in program memory or table memory and to save the address bits used for the Stallings's system.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Leach et al.'689 discloses: a data processing with instruction cache. In the event that the desired address mode is a post-index or post-displacement add or subtract, controller 14 will cause multiplexer 84 to select auxiliary register bus 65a to be connected to address lines 30a of data bus 30 (corresponding to the operation "add=ARn" in Tables 1 and 2). Conversely, if the desired indirect address mode is a pre-index or pre-displacement indirect address, controller 14 will cause multiplexer 84 to select the output of adder/subtractor 80 for application to

address lines 30a of data bus 30 (corresponding to the operation "add=ARn+/-IRm/disp" in Tables 1 and 2). Brechard et al.'778 discloses: an algebraic coder-decoder for Reed Solomon and BCH block codes, applicable to telecommunications. The indirect memory access automation includes in addition to counters 521 and 531 and the associated status flip flops 512 and 513, an unsigned 8 bit adder 560 whose output is connected to the input counters 521 and 531.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

8. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
September 15, 2004